Hall Ticket Number:

Code No.: 21502

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
B.E. II Year (I.T.) I – Semester (Main) Examinations, December – 2015

Micro Electronics

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

Part-A (10 X 2=20 Marks)

1. Determine the number of free electrons and holes in a sample of silicon which is doped with 4 $x10^{14}$ donor atoms/cm^3. The intrinsic concentration is $2.5X10^8$ / cm^3
2. Calculate the currents in the circuits shown in Fig.1 R=1K

Fig. 1

3. Using potential barrier diagram define 'Early effect'.
4. How transistor can be used as a switch?
5. Why FET is called a unipolar device?
6. Define noise margins.
7. What are the advantages of negative feedback in an amplifiers?
8. What are the advantages of crystal oscillators?
9. What are the ideal characteristics of Operational Amplifier?
10. Draw the Integrator circuit diagram using Operational Amplifier.

Part-B (5 X 10=50 Marks)

11. a) Draw the circuit diagram of full wave rectifier and derive the equation for ripple factor, average vvoltage, rms voltage and efficiency. [6]

    b) Derive an expression for the contact or barrier potential of an open-circuited p-n junction diode. [4]

Contd…2

12. a) Draw the Common Emitter Configuration circuit diagram, input and output characteristics and from the characteristics, how to find h- parameters? [5]
    b) Design a fixed bias circuit shown in Fig.2 so that V_{CE} =4V and I_C=3mA. The Supply voltage V_{cc} =12V, V_{BB} =3V and the transistor β is 125. Assume V_{BE} =0.6V [5]

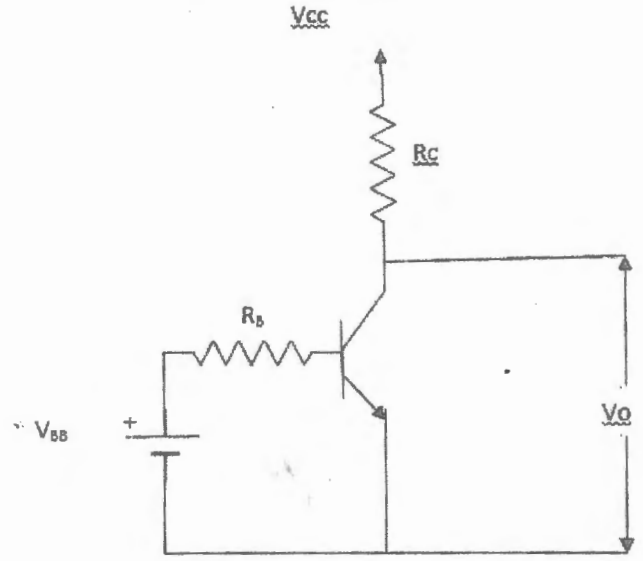

Fig. 2

13. a) Draw a typical drain characteristics for an n-channel JFET. Identify the regions and indicate important current and voltage levels. [5]
    b) Design a two input NAND gate using CMOS logic and explain its working with the help of truth table. [5]

14. a) Derive an equation for the input impedance and output impedance of an amplifier that uses series voltage negative feedback. [5]
    b) Explain how Hartley oscillators are used to generate oscillations? [5]

15. a) Draw a circuit diagram using Operational Amplifier to generate square wave and derive the equation for its frequency of oscillation. [5]
    b) Design a circuit using Operational Amplifier for V_o= -(2V_1+3V_2). Assume the smallest resistance value as 10K. [5]

15. a) Draw the V-I characteristics of zener diode and explain how a zener diode is used as regulator? [5]
    b) What is the effect of emitter by pass capacitor in CE amplifier? [5]

16. Write short notes on any **two** of the following:
    a) Complex CMOS logic gates design [5]
    b) Class B power amplifier [5]
    c) Operational Amplifier as logarithmic amplifier [5]

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